

P A T E N T

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Fiorella et al.

Application No.:

Filed: Herewith

For: **METHODS AND APPARATUS FOR UPGRADING FIRMWARE IN AN EMBEDDED  
SYSTEM**



**DRAWING REVIEW BRANCH**

Commissioner for Patents  
Washington, D.C. 20231

**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as Express Mail (No. EL 628667881 US) addressed to BOX PATENT APPLICATION, Commissioner for Patents, Washington, D.C. 20231 on March 14, 2001.

By: Michele Hollis  
Michele Hollis

**TRANSMITTAL OF FORMAL DRAWINGS**

Dear Sir:

Enclosed are three (3) sheets of formal drawings for filing in the above-referenced patent application.

Please advise the undersigned attorney if correction is necessary.

Respectfully submitted,

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**ATTORNEY DOCKET NO.: GIC-632**

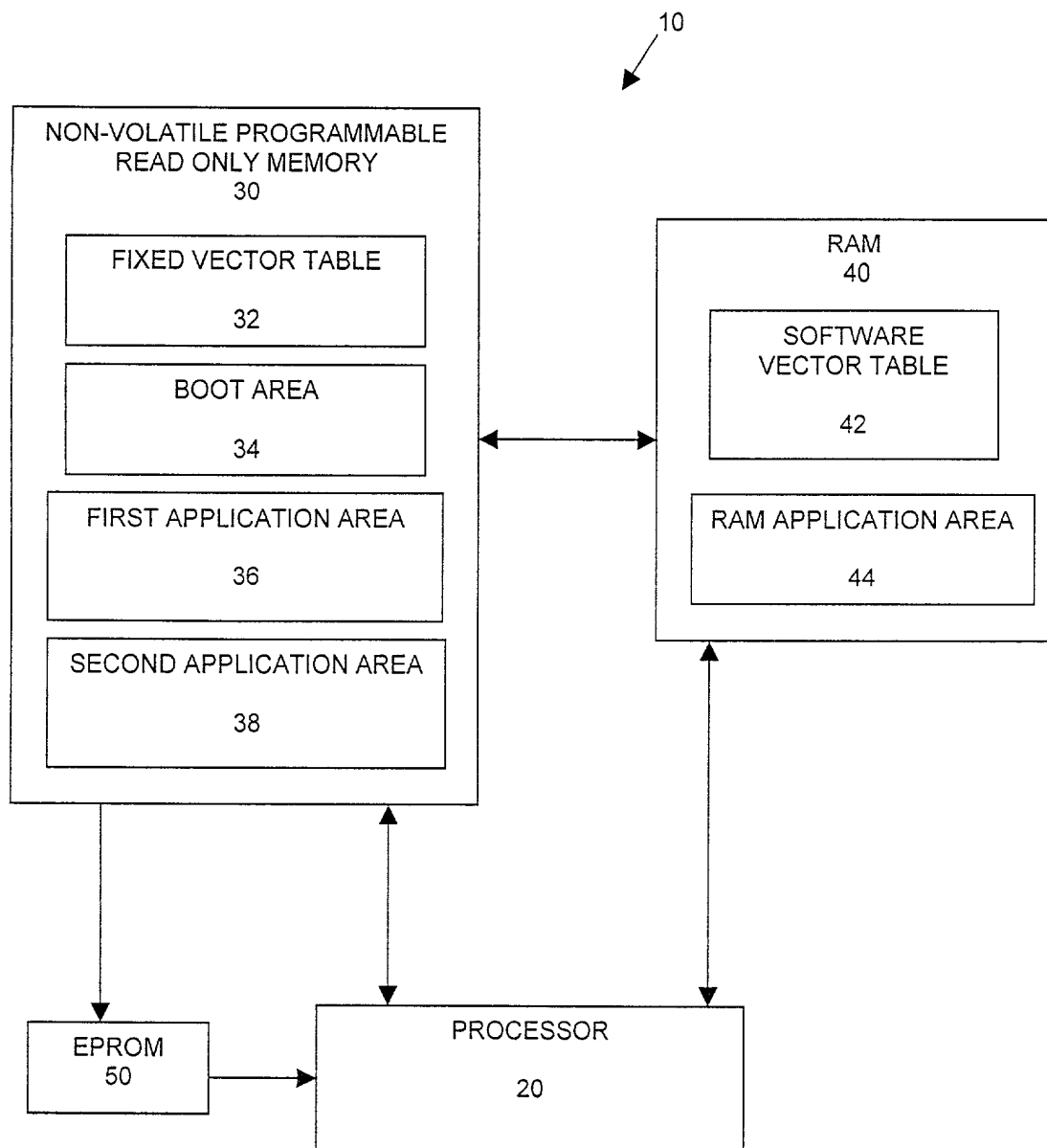


FIG. 1

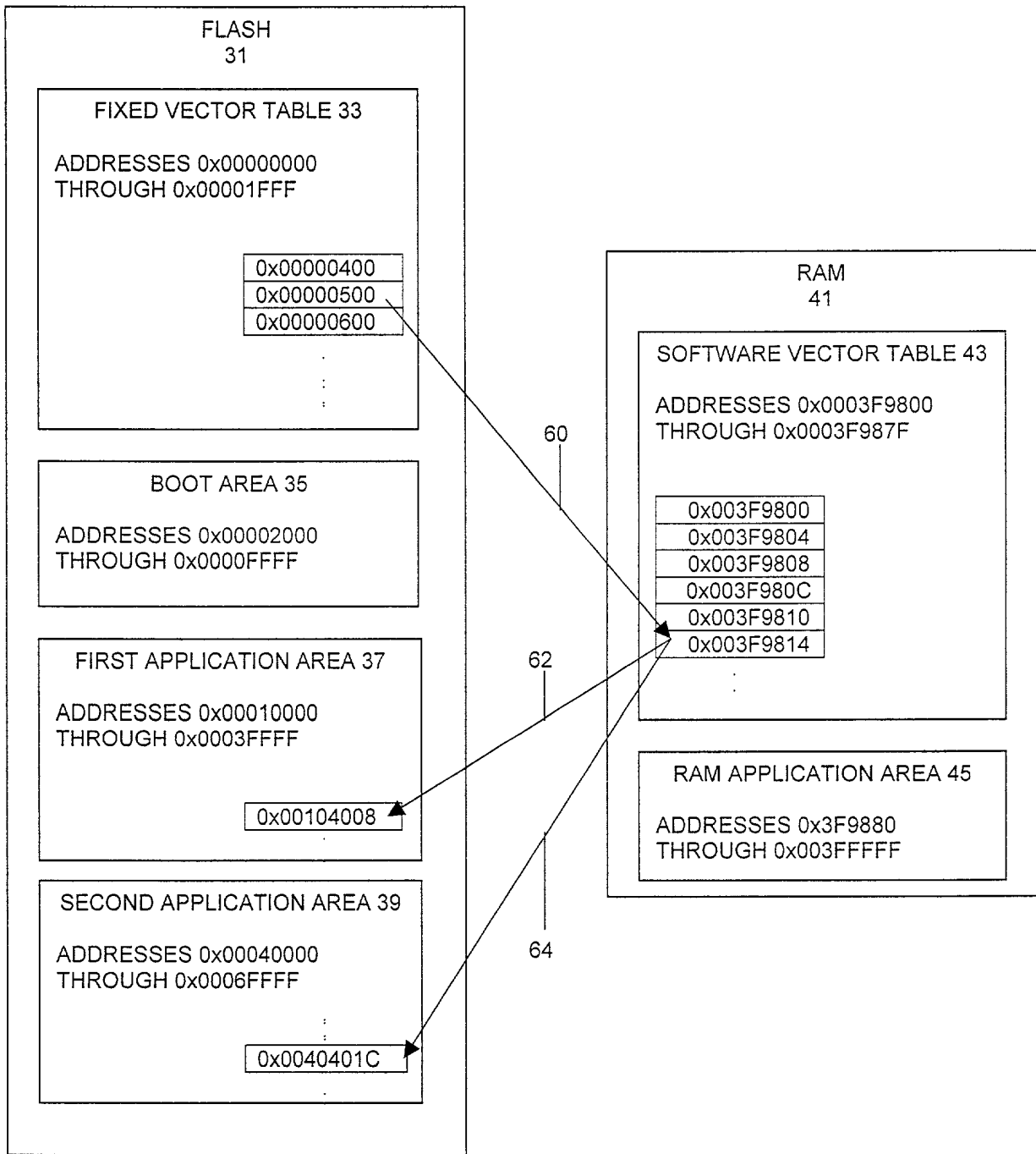
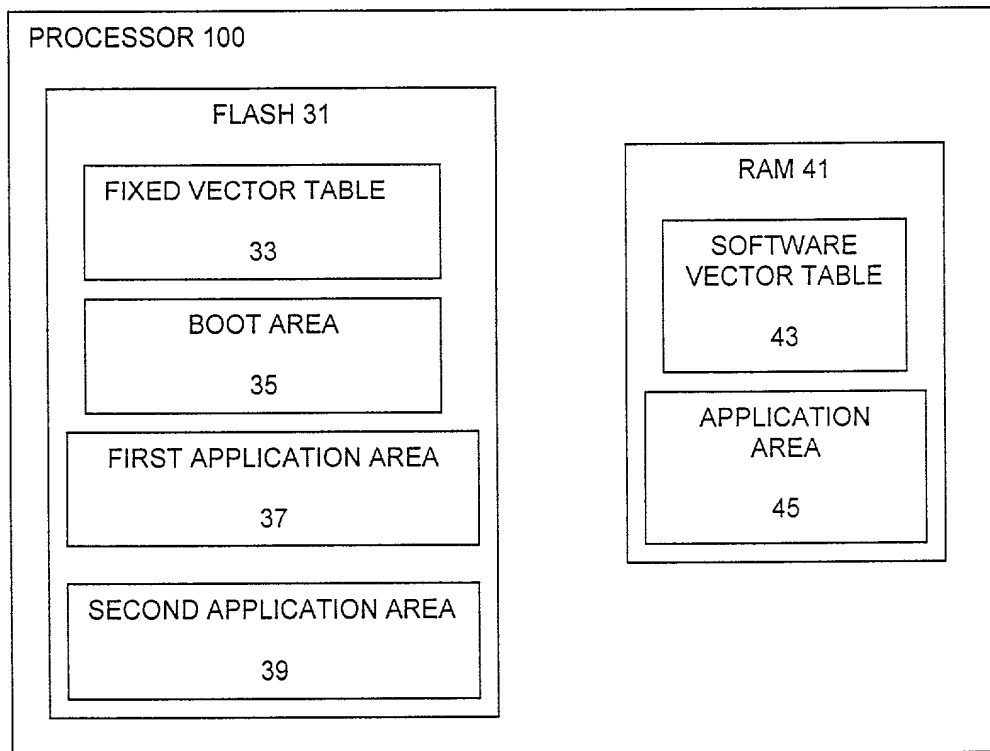


FIG. 2

FIG. 3 is a block diagram of a processor 100, showing the internal structure of the processor. The processor 100 includes a FLASH 31 and a RAM 41. The FLASH 31 is divided into a FIXED VECTOR TABLE 33, a BOOT AREA 35, a FIRST APPLICATION AREA 37, and a SECOND APPLICATION AREA 39. The RAM 41 is divided into a SOFTWARE VECTOR TABLE 43 and an APPLICATION AREA 45.



**FIG. 3**